WHAT IS CLAIMED IS:-

1. An edge correcting circuit of an image to be represented by a digitized image signal, comprising:

a high-frequency signal extracting circuit for extracting a high-frequency signal of the image by calculation based on a signal of a pixel which is to be corrected (hereinafter called a target pixel), a signal of a pixel shifted from the target pixel by m (m being an integer not smaller than 2) pixels in the right or lower direction, and a signal of a pixel shifted from the target pixel by m pixels in the left or upper direction;

an amplitude-restricting signal generator for determining an amplitude-restricting signal based on a minimum value or a maximum value of an absolute value of a difference between the signal of the target pixel and a signal of a pixel shifted from the target pixel by n (n being an integer not smaller than 1 and smaller than m) pixels in the right or lower direction, and an absolute value of a difference between the signal of the target pixel and a signal of a pixel shifted from the target pixel by n pixels in the left or upper direction;

an amplitude restricting circuit for restricting the output of the high-frequency extracting circuit so that the absolute value of the output of the high-frequency extracting circuit is not more than the output of the amplitude-restricting signal generator; and

an adder for adding the output of the amplitude restricting circuit or a signal obtained therefrom, as an edge correction signal, to the signal of the target pixel.

2. The edge correcting circuit as set forth in claim 1, wherein said high-frequency extracting circuit has the function of altering the amplitude of the high-frequency signal output therefrom.

3. The edge correcting circuit as set forth in claim 1, wherein

said amplitude-restricting signal generator has the function of altering the amplitude of the amplitude-restricting signal output therefrom.

4. The edge correcting circuit as set forth in claim 1, further comprising:

a subtractor for subtracting the output of the amplitude restricting circuit from the output of the high-frequency extracting circuit;

an amplitude control circuit for controlling the amplitude of the output of the subtractor; and

a second adder for adding the output of the amplitude control circuit and the output of the amplitude restricting circuit;

wherein the output of the second adder is used as the edge correction signal.

5. The edge correcting circuit as set forth in claim 1, further comprising:

a subtractor for subtracting the output of the amplitude restricting circuit from the output of the high-frequency extracting circuit;

an amplitude adjusting circuit for adjusting the amplitude of the output of the amplitude restricting circuit; and

a second adder for adding the output of the subtractor and the output of the amplitude adjusting circuit;

wherein the output of the second adder is used as said edge correction signal.

6. An edge correcting circuit of an image to be represented by a digitized image signal, comprising:

a high-frequency signal extracting circuit for extracting a high-frequency signal of the image by calculation based on a signal of a pixel which is to be corrected (hereinafter called a target pixel), a signal of a pixel shifted from the target pixel by m (m being an integer not smaller than 2) pixels in

the right or lower direction, and a signal of a pixel shifted from the target pixel by m pixels in the left or upper direction;

an amplitude-restricting signal generator for determining an amplitude-restricting signal based on a difference between the signal of the target pixel and a signal of a pixel shifted from the target pixel by n (n being an integer not smaller than 1 and smaller than m) pixels in the right or lower direction, and a difference between the signal of the target pixel and a signal of a pixel shifted from the target pixel by n pixels in the left or upper direction;

an amplitude restricting circuit for restricting the output of the high-frequency extracting circuit so that the absolute value of the output of the high-frequency extracting circuit is not more than the output of the amplitude-restricting signal generator; and

an adder for adding the output of the amplitude restricting circuit or a signal obtained therefrom, as an edge correction signal, to the signal of the target pixel;

wherein

said amplitude-restricting signal generator outputs "0" when a first difference value obtained by subtracting the signal of the target pixel from the signal of the pixel shifted by n pixels from the target pixel in the right or lower direction, and a second difference value obtained by subtracting the signal of the target pixel from the signal of the pixel shifted by n pixels from the target pixel in the left or upper direction are of the same sign (or at least one of them is zero), and

said amplitude-restricting signal generator selectively outputs that one of the first and second difference values which is of the same sign as the output of the high-frequency extracting circuit, when neither of the first and second difference values is zero, and the first and second difference values have different signs.

7. The edge correcting circuit as set forth in claim 6, wherein

said high-frequency extracting circuit has the function of altering the amplitude of the high-frequency signal output therefrom.

8. The edge correcting circuit as set forth in claim 6, wherein said amplitude-restricting signal generator has the function of altering the amplitude of the amplitude-restricting signal output therefrom.

9. The edge correcting circuit as set forth in claim 6, further comprising:

a subtractor for subtracting the output of the amplitude restricting circuit from the output of the high-frequency extracting circuit;

an amplitude control circuit for controlling the amplitude of the output of the subtractor; and

a second adder for adding the output of the amplitude control circuit and the output of the amplitude restricting circuit;

wherein the output of the second adder is used as the edge correction signal.

10. The edge correcting circuit as set forth in claim 6, further comprising:

a subtractor for subtracting the output of the amplitude restricting circuit from the output of the high-frequency extracting circuit;

an amplitude adjusting circuit for adjusting the amplitude of the output of the amplitude restricting circuit; and

a second adder for adding the output of the subtractor and the output of the amplitude adjusting circuit;

wherein the output of the second adder is used as said edge correction signal.